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Terms	Documents
L1 same device same current	15

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L7

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Search History

DATE: Thursday, August 05, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L7	L1 same device same current	15	L7
L6	L5 same internal	14	L6
L5	L1 same l3	51	L5
L4	L3 same l2	7	L4
L3	semiconductor or (integrated adj1 circuit) or ic or chip	2667863	L3
L2	L1 same current	50	L2
L1	self-test same (power adj1 supply)	271	L1

END OF SEARCH HISTORY

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L4: Entry 4 of 7 File: JPAB Dec 18, 2002

DOCUMENT-IDENTIFIER: JP 2002365336 A
TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND TESTING DEVICE

Abstract Text (2):
SOLUTION: This semiconductor integrated circuit device 1000 comprises internal power supply circuits 200, 210 and 230 provided each between a prescribed internal circuit of two or more internal circuits 100.1-100.9 and a power supply wiring VCL for converting the level of an external power source potential to supply an internal power source potential to the prescribed internal circuit; and a control circuit 20 for performing the self-test of the semiconductor integrated circuit device. The control circuit 20 detects the current quantity supplied to the prescribed internal circuit by the internal power supply circuit, and a data input and output part 30 outputs the detection result to the outside.

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L7: Entry 13 of 15 File: DWPI Jun 17, 2003

DERWENT-ACC-NO: 2003-493631
DERWENT-WEEK: 200419

TITLE: Monitoring and testing method for battery of a hazardous condition alarm device when both primary and standby battery power supplies are available, stand-by battery supplies current when the alarm device is in self-test mode

Basic Abstract Text (1):
NOVELTY - The method involves testing the battery of a hazardous condition alarm device in which the alarm device is powered by a primary power supply. The alarm device has a stand-by battery power supply and is operable in a self-test mode, an alarm mode and a quiescent mode. The current drain in self-test and alarm modes exceeds a quiescent current drain. The method includes switching the current supplied by the primary power supply and the stand-by battery power supply such that, when both the primary and standby battery power supplies are available, the stand-by battery supplies current when the alarm device is in self-test mode and not when the alarm device is in quiescent mode.

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L7: Entry 9 of 15 File: EPAB Jun 12, 2003

DOCUMENT-IDENTIFIER: WO 3048796 A1
TITLE: BATTERY TESTING METHOD FOR HAZARDOUS CONDITION ALARM DEVICES AND SYSTEMS

Abstract Text (1):
CHG DATE=20030902 STATUS=O>A method of monitoring and testing the battery of a hazardous condition alarm device in which the alarm device is powered by a primary power supply, the alarm device having a stand-by battery power supply and being operable in a self-test mode, an alarm mode and a quiescent mode, the current drain in self-test and alarm modes exceeding the quiescent current drain, the method including: switching the currents supplied by the primary power supply and the stand-by battery power supply such that, when both the primary power supply and the stand-by battery power supply are available, the stand-by battery supplies current when the alarm device is in self-test mode and not when the alarm device is in quiescent mode.

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L6: Entry 4 of 14 File: USPT Apr 20, 1993

DOCUMENT-IDENTIFIER: US 5203867 A
TITLE: Method for generating power-up pulse

Brief Summary Text (3):
In many cases, an integrated circuit device includes logic or other circuits that must be preset or inhibited while the device is being powered up to an external power supply. A "power-up" circuit is used to generate an internal signal for presetting or inhibiting logic or other circuits and may also be used for other purposes such as triggering on-chip self-test functions. The power-up circuit must reliably detect application of voltage to the chip, whether energized rapidly or slowly.

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L6: Entry 5 of 14 File: USPT Jul 9, 1991

DOCUMENT-IDENTIFIER: US 5030845 A
TITLE: Power-up pulse generator circuit

Brief Summary Text (3):
In many cases, an integrated circuit device includes logic or other circuits that must be preset or inhibited while the device is being powered up by an external power supply. A "power-up" circuit is used to generate an internal signal for presetting or inhibiting logic or other circuits and may also be used for other purposes such as triggering on-chip self-test functions. The power-up circuit must reliably detect application of voltage to the chip, whether energized rapidly or slowly.

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L6: Entry 7 of 14 File: USPT Mar 21, 1989

DOCUMENT-IDENTIFIER: US 4814712 A
TITLE: Test kit for a circuit breaker containing an electronic trip unit

Detailed Description Text (8):
The operation of the test kit 20 (FIG. 2), for obtaining status and trip information from an integrated circuit breaker 10 by operation of the test circuit 30 generally described in FIG. 3, is depicted in the flow chart 130 in FIG. 7. For purposes of illustration, the integrated circuit breaker 10 of FIG. 2 is connected with the test kit by means of the analog test jack access opening 25 when the trip unit contains an analog signal processor and internal electrical connection is made with the analog trip circuit 44 shown in FIG. 5B by means of the analog test jack circuit 119. When a digital signal processor is contained within the trip unit of the integrated circuit breaker 10, the test kit becomes connected with the integrated circuit breaker by insertion of the test plug connector 26 within the separate digital test jack access opening 134. Internal connection is then made with the digital test jack circuit 118 contained within the power supply output circuit 31B shown in FIG. 5B. The test functions are initiated by pressing any of the appropriate buttons 23B on the test kit enclosure as shown in the flow chart format of FIG. 7. Upon power-up, the microcomputer 29 within the test kit circuit 30 of FIG. 3 performs a variety of self-test functions (121) similar to that described in the aforementioned U.S. patent application Ser. No. 626,341. The operation of the test kit is best understood by referring to both FIG. 3 and FIG. 7. Should the test kit fail the self-test (122), the failure mode is displayed (123) on the LCD 22 to alert the operator. Should the test kit pass the self-test (122), the status of the test kit (124) is displayed on the LCD 22. The operator at this time can then enter any of a plurality of functions by pressing the corresponding operation button 23B. One function being the display of the switch settings and options (125) contained within the integrated circuit breaker trip unit. Should the operator initiate a trip unit self-test (126) by pressing the designated button 23B the trip unit immediately performs a self-test and displays the results (131) on the LCD. Depressing another designated button 23B causes the test kit 20 to simulate an over-current condition (127) within the integrated circuit breaker optionally causing the integrated circuit breaker to trip (132). Another designated button 23B instructs the integrated circuit breaker trip unit to display selected pick-up and trip values (128) on the LCD. Another designated button 23B allows the operator to directly trip the integrated circuit breaker (129).

US006532183B2

(12) **United States Patent**
Ooishi

(10) **Patent No.: US 6,532,183 B2**
(45) **Date of Patent: Mar. 11, 2003**

(54) **SEMICONDUCTOR DEVICE CAPABLE OF ADJUSTING INTERNAL POTENTIAL**

(75) Inventor: **Tsukasa Ooishi**, Hyogo (JP)

(73) Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/983,075**

(22) Filed: **Oct. 23, 2001**

(65) **Prior Publication Data**

US 2002/0186602 A1 Dec. 12, 2002

(30) **Foreign Application Priority Data**

Jun. 11, 2001 (JP) 2001-176032

(51) **Int. Cl.**[7] **G11C 7/00**
(52) **U.S. Cl.** **365/201**; 365/226
(58) **Field of Search** 365/201, 226, 365/227; 327/379, 315, 317, 538, 543

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"A Programmable BIST Core for Embedded DRAM", Chih-Tsun Hung Et Al., IEEE Design & Test of Computers, Jan.-Mar. 1999, pp. 59-69.

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Primary Examiner—Michael S. Lebentritt
Assistant Examiner—Ann Phung
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A system LSI comprises a signal generation circuit supplying 16 level set signals one by one to an internal power supply potential generation circuit to increase an internal power supply potential in 16 stages, a compare circuit comparing each internal power supply potential with a reference potential and outputting a signal of a level responsive to the result of comparison and a memory circuit temporarily storing the signal output from the compare circuit. Therefore, an optimum level set signal can be readily detected on the basis of an output signal from the memory circuit.

19 Claims, 18 Drawing Sheets